

**In the Claims:**

Please cancel claims 12-19. Please amend claims 1-2, 5, 7-8, and 10. Please add new claims 20-28. The claims are as follows.

1. (Currently amended) A method of testing a semiconductor chip having a plurality of common I/Os associated therewith whose characteristics or properties may be tested by applying a test signal through a control I/O, the method comprising the steps of:

~~performing~~ connectivity testing a chip-to-package ~~connectivity test upon connection of~~ at least one of the common I/O through the control I/O; and

determining whether the ~~common I/O~~ chip-to-package connection is faulty from a result of the ~~chip-to-package~~ connectivity testing.

2. (Currently amended) The method of claim 1, wherein ~~performing a pin-to-package~~ the connectivity testing comprises:

launching a transition through the common I/O to an associated I/O package connection and pad; and

observing a response of the transition.

3. (Original) The method of claim 2, further comprising: triggering a first latch at an initialization of the transition response and triggering a second latch when the transition response has reached a transition threshold value.

4. (Original) The method of claim 3, wherein determining whether the chip-to-package connection is faulty comprises: comparing a difference between values stored in association with the first and second latches.

5. (Currently amended) The method of claim 1, wherein determining whether the chip-to-package connection is faulty comprises: comparing a first RC constant associated with a first signal relating to a connectivity testing of a first I/O with a second RC constant associated with a second signal relating to a connectivity testing of a second I/O.

6. (Original) The method of claim 5, further comprising identifying the first I/O as having a faulty connection if the first RC constant is greater than the second RC constant.

7. (Currently amended) The method of claim 1, wherein performing ~~the chip-to-package~~ connectivity testing comprises generating a transition signal from a driver of the common I/O, wherein the driver is configured as a weak driver that is sensitive to capacitive loading.

8. (Currently amended) The method of claim 7, wherein ~~generating the transition from the weak driver comprises~~ further comprising placing an additional impedance into connection with the driver prior to ~~launching~~ generating the transition signal.

9. (Original) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a resistor into series connection with the driver.

10. (Currently amended) The method of claim 8, further comprising electrically shorting the additional impedance from connection with the driver after ~~launching~~ generating the transition signal.

11. (Original) The method of claim 10, wherein electrically shorting the additional impedance includes completing a circuit around the additional impedance to bypass the additional impedance.

20. (New) The method of claim 9, wherein the resistor has an electrical resistance of at least 1 k $\Omega$ .

21. (New) The method of claim 9, wherein the resistor has an electrical resistance of at least 10 k $\Omega$ .

22. (New) The method of claim 9, wherein the resistor has an electrical resistance of at least 35 k $\Omega$ .

23. (New) The method of claim 9, wherein the resistor is electrically interposed between the driver and the common I/O.

24. (New) The method of claim 8, wherein placing an additional impedance into connection with the driver comprises placing a field effect transistor (FET) into series connection with the driver.

25. (New) The method of claim 24, wherein the FET is electrically interposed between the driver and the common I/O.

26. (New) The method of claim 8, wherein the additional impedance is electrically interposed between the driver and the common I/O.

27. (New) The method of claim 7, further comprising providing semiconductor circuitry between the driver and the control I/O.

28. (New) The method of claim 27, wherein the semiconductor circuitry includes at least one of a clock tree, a latch, and a receiver.